A High Performance K-Band Diplexer using High-Q Micromachined Cavities

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Abstract

Microwave diplexers are often used on transmit / receive systems to isolate a power transmit stage from a sensitive receive stage sharing a common antenna. With the ever-increasing need for efficient bandwidth usage, diplexers exhibiting close channel spacing, low insertion loss and small channel bandwidths are increasingly necessary. Utilizing two high Q cavity resonators, a Duroid-based high performance diplexer has been designed, fabricated and measured. This diplexer shows transmit / receive bandwidths of 2.39% and 1.8% and insertion losses of 2.38dB and 2.89dB, respectively. Channel center frequencies of 18.8GHz and 20.7GHz provide a channel separation of approximately 9% and channel to channel isolation greater than 24dB. Utilizing machined aluminum cavities and a Duroid substrate the diplexer design provides insight into cavity based diplexer construction, allowing for the design of a silicon based micromachined cavity diplexer. Simulation results from this silicon-based diplexer are also presented.

Index Terms – Diplexer, Laser Micromachined, Cavity Resonator, K-Band.

Introduction

With the rapid expansion and growth of wireless communication systems for military and commercial applications, implementation of microwave and mm-wave systems is increasing dramatically due to their advantages over conventional architectures. Commercial applications of these systems include short-haul line-of-sight transmission links for personal communication networks (PCNs) that operate at 38 GHz, wireless cable at 28 GHz, wireless local area networks (LANs), automotive anti-collision radar at 77 GHz and mobile broadband systems [1]. Microwave and millimeter-wave components are traditionally built with waveguide technology that offers low-loss and high quality factor circuits at the price of large size and weight, high cost, incompatibility with monolithic circuits and increased fabrication complexity especially at higher frequencies [2]. For commercial systems, however, high yield, increased component density and low cost are fundamental requirements that need to be met.

One of the major limiting waveguide components of microwave/mm-wave wireless communication systems is the transmit/receive diplexer that is used to provide low-insertion loss and high channel-to-channel isolation. Realization of the diplexer with planar resonators and filters is generally avoided due to the low quality factor and higher losses of those circuits that are caused by the presence of the substrate material. With the recent developments, however, in microwave micromachining it is now possible to make microstrip or CPW line resonators suspended on membrane [3], [4], as well as cavity resonators [5] and dielectric resonators [6] that offer low-loss, high-Q and narrow bandwidth and can be monolithically integrated with other passive components and active devices on a single chip. These advances have led to the development of high performance, suspended microstrip based K-band diplexers exhibiting 5%-6.5% bandwidths and 0.9 dB – 1.4 dB insertion loss [3]. This paper will present a new diplexer design based on silicon laser micromachined cavity resonators.

Cavity Design

Microstrip coupled resonant filters have been shown to provide high-Q filtering at microwave frequencies [2]. Because of the performance and ease of integration of these filters, they are ideally suited for use in frequency selective diplexers. The diplexer in this paper is designed around two microstrip coupled resonant cavities. Because of the recent interest in the use of the K-band for point to point communications and wireless LANs [7], 19 GHz and 21 GHz were selected for the diplexer design. Using equation (1),

$$f_{res} = \frac{c}{2p}\sqrt{\left(\frac{p}{L}\right)^2 + \left(\frac{p}{W}\right)^2} \qquad (1)$$

the width and length for two rectangular TE_{101} resonant cavities were found to be [8]: W=8.01mm, L=17.5mm and W=8.85mm, L=15.83mm for the A and B cavities, respectively. For each of these cavities, the unloaded Q at resonance is governed mainly by the height of the cavity [2]. In this case a height of 0.93mm was chosen. This height provides theoretical unloaded Q's of approximately 1321 and

1366. Additionally, this height allows the cavity to be constructed in 2 sandwiched 0.5mm thick silicon wafers.

Using the cavity filter layout strategies of Papapolymerou [2], the transmit and receive filters of the diplexer were designed independently (see Figure 1 for a picture of a single cavity).

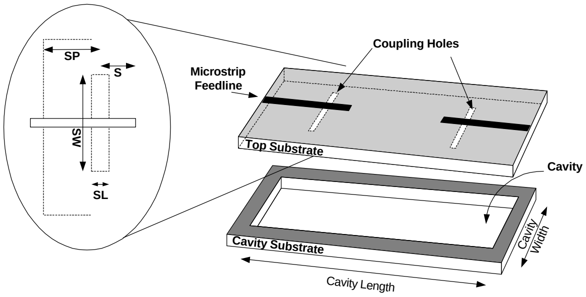

Figure 1: Microstrip coupled cavity

For testing purposes, the initial design of these cavities utilized a Duroid substrate. This substrate has a relative dielectric constant of 10.8, which is reasonably similar to silicon (11.7). Because this substrate supports the input and output feed microstrips to the cavities, it has very little impact on the operation of the cavity filter itself. In order to use a top substrate with a different dielectric constant (say silicon), one has to readjust the input and output microstrip widths to provide 50 Ω line impedance. The other filter dimensions remain largely unchanged. Because of physical layout limitations, this fact may prove extremely useful in future work, and will be discussed in more detail later in this paper.

Following the rough design of the cavity dimensions, the cavity structures were modeled in Ansoft's High Frequency Structure Simulator (HFSS). HFSS modeling allows the cavity performance to be simulated and optimized. A scripting language provided in HFSS allows the user to vary structure parameters, like the input and output stub lengths, simulate, and store the simulation results without further user intervention. Because the runtime of each cavity simulation can be as much as 12 hours, this scripting capability makes parameter sweeps and optimizations significantly more efficient. Using this method, the initial cavity parameters were adjusted to improve the performance of each cavity. The simulated response (S21) of each cavity is shown in Figure 2.

These results show a 1.3% bandwidth and 0.26 dB of insertion loss for the 19GHz cavity. The 21GHz cavity yielded 1.3% bandwidth and 0.27 dB of insertion loss.

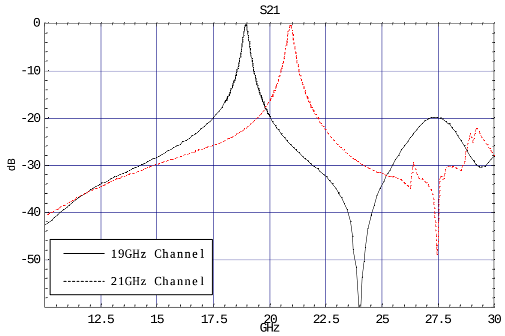

Figure 2: Simulated Cavity Response

Diplexer Design

With the cavity simulations completed, the two cavities were combined into one HFSS simulation, along with a 'T' feed network (see Figure 3). For proper diplexer operation, it is important that the lengths L1 and L2 be adjusted so that at the resonant frequency of F1, the input to F2 looks like an open circuit at the T junction. Similarly, at the resonant frequency of F2, the input to F1 should look like an open circuit at the T junction. Neglecting open-end and cavity effects, one would ideally design L1 and L2 to be approximately $\lambda_{gres2}/2$ and $\lambda_{gres1}/2$, respectively. However, this is not always possible. Because the physical length of the half wavelength stubs depend on the relative dielectric constant of the substrate, it is possible that with high ε_r substrates (physically short $\lambda_g/2$'s), the cavities beneath the microstrips will collide (d will approach 0). When designing the cavity, it is important that the coupling slot be located approximately ¼ of the cavity length from the cavity edge, and for proper coupling it is necessary to have a $¼\lambda_g$ stub beyond the center of the coupling slot [2]. For physically realizable designs, these two constraints result in an upper limit on the dielectric constant of the microstrip substrate

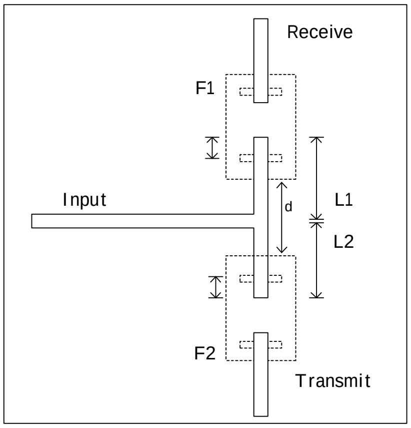

Figure 3: Diplexer Schematic

It can be shown that for physically realizable designs, both cavity resonators must satisfy equation (2),

$$\sqrt{e_e} < \frac{4c}{L_{cavity1}+4d_{\min}}\left(\frac{1}{2\,f_{res2}}-\frac{1}{4\,f_{res1}}\right) \qquad (2)$$

where:

ε_e is the effective dielectric constant of the microstrip lines,

c is the speed of light,

$L_{cavity1}$ is the length of the first cavity

f_{res1} and f_{res2} are the resonant frequencies of the first and second cavities respectively,

d_{min} is the minimum manufacturable distance between the two cavities.

One solution to this problem is to allow L1 & L2 to be larger than $\lambda_g/2$. Any length $n\lambda_g/2$ will reflect as an open circuit at the T-junction, and should allow proper operation of the junction. However, for n>0, L1 and L2 will reflect open circuits to the T junction at frequencies other than the resonant frequency of the cavity resonators. Ripples in the response of the diplexer will result in this case. These ripples can be severe, and as n gets large, can begin to overlap the cavity resonance, resulting in very poor performance.

In this design it was found that the cavities would overlap if L1 and L2 were $\lambda_{g2}/2$ and $\lambda_{g1}/2$ respectively, and that setting L1 and L2 to λ_{g2} and λ_{g1} (n=2) provides an acceptable balance between a non-physical solution (cavity overlap) and good performance. These lengths were then optimized in HFSS to account for parasitics and open end effects.

Future designs may utilize a dielectric loaded cavity, which will reduce the size of the cavity. This will relax the constraint imposed by equation (2), by reducing L_{cavity} significantly.

Fabrication

The cavity diplexer was fabricated using standard circuit board processing techniques on Rogers Duroid (ε_r=10.8). This circuit board was mounted on top of an aluminum support fixture. The cavities for the two filters were machined into the fixture. The design dimensions for the two cavities are shown in Table 1.

For proper performance of the diplexer, the location of the coupling slots with respect to the cavity walls must be properly maintained. In order to accurately align the aluminum fixture to the circuit board, small holes were machined in the aluminum fixture containing the cavities. A matched set of holes was drilled in the Duroid circuit, using a printed pattern on the board to automatically center the drill bit. The two pieces were then aligned with a gauge pin, and clamped together. To ensure good diplexer performance and minimize losses, 12 screws and a clamp were used to secure the circuit board to the fixture.

Dimension (refer to Figure 1)	Cavity 1	Cavity 2
f_{res}	18.99GHz	20.99GHz
Cavity Length	17.50mm	15.83mm
Cavity Width	8.85mm	8.01mm
Cavity Height	0.93mm	0.93mm
Top Substrate Thickness	0.635mm	0.635mm
Top Substrate εr	10.8	10.8
Microstrip width	0.56mm	0.56mm
S	0.96mm	0.87mm
SP	4.40mm	3.98mm
SW	3.48mm	3.15mm
SL	0.34mm	0.31mm

Table 1 : Diplexer Dimensions

Measurements

The assembled diplexer was characterized using an HP8510 network analyzer. The network analyzer was calibrated, and the S-Parameters for the diplexer were measured. Additionally, a thru section of line was measured to allow both the fixture and line loss of the diplexer to be de-embedded. Both the simulated and measured data are shown in Figures 4 and 5.

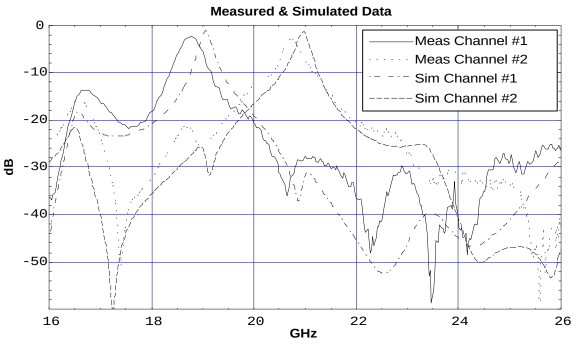

Figure 4: Measured and Simulated Data

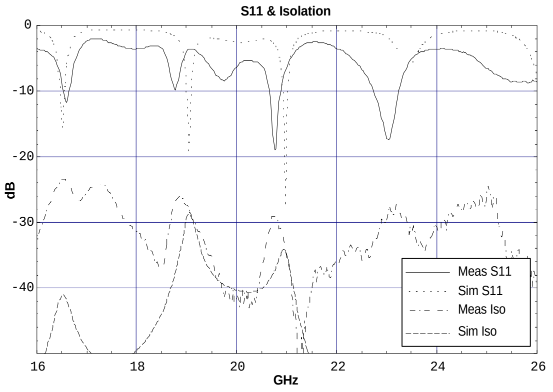

Figure 5: Input Match & Isolation

At the channel centers, the diplexer exhibits an insertion loss of 2.38 dB and 2.89 dB for the transmit and receive channels respectively. The measured isolation was better than 24 dB at all frequencies measured. Channel bandwidth measurements show 2.39% and 1.8% bandwidth for the transmit and receive channels, respectively. Comparison of the measured data with simulation results in Table 2 show some differences.

	Measured		Simulated		
	Transmit	**Receive**	**Transmit**	**Receive**	**Ave Δ**
BW	2.39%	1.80%	1.25%	1.27%	66%
Center Freq.	18.78 GHz	20.73 GHz	19.06 GHz	20.96 GHz	1.3%
Insertion loss at peak	2.38dB	2.89dB	1.24dB	1.43dB	1.3dB

Table 2: Measured Vs. Simulated Results

The most significant difference shown in these data is the channel bandwidth comparison. It is believed that manufacturing and assembly issues such as surface roughness, and contact resistance between the aluminum cavity and the circuit board ground plane are reducing the Q of the resonant cavities, resulting in wider than expected bandwidths. With IC fabrication techniques for the silicon diplexer and more fine tuning, it is expected that the measured insertion loss and bandwidths could be improved.

Silicon Diplexer

Following the design of the Duroid model, a silicon-based diplexer was designed. In this diplexer, the Duroid is replaced with a high resistivity silicon wafer. The cavities are created in silicon by a laser ablation technique. This yields vertical cavity walls, with the cavities residing in two sandwiched 0.5mm wafers. The cavity surfaces are then metalized with the use of an e-beam evaporator. The top wafer and the cavity assembly are glued together using conductive epoxy.

The simulated results for the silicon-based diplexer are shown in Figure 6. The results of these simulations indicate comparable performance to the Duroid based diplexer.

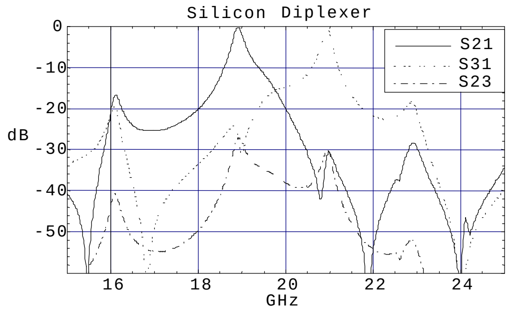

Figure 6: Simulated Silicon Diplexer

Currently, the silicon-based diplexer is being fabricated for testing. Because silicon processing offers more accurate alignment, higher lithography resolution and better bonding between the circuit wafer and cavity, it is likely that the silicon diplexer will outperform the Duroid diplexer.

Conclusions

Microstrip coupled resonant cavity diplexers can exhibit good performance if properly designed. Because these diplexers are easy to integrate with microstrip based circuits they are well suited for wireless design. A novel Duroid based diplexer has been demonstrated which shows very good performance compared to other state-of-the-art integrated diplexers. The simulations of this diplexer agree well with the measured results. Work is in progress on a silicon-based diplexer with comparable performance.

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